



ATTORNEY DOCKET NO. 03-LJ-011
U.S. SERIAL NO. 10/604,964
PATENT

DOCKET NO. 03-LJ-011 (STMI01-03011)
Customer No. 30425

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : Razak Hossain
Serial No. : 10/604,964
Filed : August 28, 2003
For : SCAN CHAIN MODIFICATION FOR REDUCED LEAKAGE
Group No. : 2825
Examiner : Naum B. Levin

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

DECLARATION OF PRIOR INVENTION UNDER 37 C.F.R. 1.131

1. This declaration is to establish prior invention in this application in the United States (or a NAFTA or WTO country), at a date prior to March 24, 2003, that is the purported effective date of the reference (Abdollahi, et al. "Leakage Current Reduction In Sequential Circuits By Modifying Scan Chain", Proceedings of the Fourth Symposium on Quality Electronic Design) cited by the U.S. Patent and Trademark Office (in the Office Action having a mailing date of November 9, 2006).

2. The person making this Declaration is the inventor, Razak Hossain.

3. To establish the date of the invention of this application, the following attached documents are submitted herewith as evidence: (1) Invention Disclosure Form (8 pages).

4. The invention in this application was conceived at least as early as March 23, 2003.

5. Upon information and belief, this Declaration is being submitted in response to a first office action issued by the United States Patent & Trademark Office.

6. As a person signing below:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE:

Inventor: Razak Hossain

Inventor Residence: 10779 SANTA TOMASA AV
SAN DIEGO, CA 92127

Inventor Country of Citizenship: USA

Inventor Signature: Razak Hossain

STMICROELECTRONICS INC.

DISCLOSURE NO. 03-LJ-011

DATE RECEIVED [REDACTED]

INVENTION DISCLOSURE FORM

COMPANY RESTRICTED WHEN COMPLETED

1. SITE: La Jolla
2. GROUP: Advanced Projects
3. DIVISION: Central R&D

4. PRODUCT CLASSIFICATION:

Technology:
System:
Circuit:

5. DESCRIPTIVE TITLE OF INVENTION (10-15 Words):

Scan Chain Modification to Support Reduced Leakage Power Dissipation

6. INVENTORS:

- a. Name: Razak Hossain
(First) (Middle) (Last)

Social Security Number: 078-74-4282

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Telephone: 858-484-7411 858-452-7715 x311
(Home) (Work)

Email: razak.hossain@st.com

Citizenship: Bangladesh

Supervisor: Naresh Soni

- b. Name:
(First) (Middle) (Last)

Social Security Number:

9. DATE AND LOCATION WHERE INVENTION WAS FIRST SUCCESSFULLY REDUCED TO PRACTICE:

.....
(Date)

.....
(Location)

Describe how invention was reduced to practice (model, on paper etc), and where model (if any) is located:

.....

10. ENGINEERING NOTEBOOK AND PAGES IN WHICH INVENTION WAS RECORDED:

.....
1988
(Notebook Number)

.....
24-26
(Page numbers)

Was each page read and witnessed by 2 persons who understood it?

Check box: ☒

11. WAS ANY OF THE WORK PERFORMED UNDER/IN-PREPARATION-OF A GOVERNMENT CONTRACT?

Yes: No: ☒

12. HAS THERE BEEN ANY:

Use of the invention by ST or others?	Yes:	No: <input checked="" type="checkbox"/>
Disclosure to others outside ST?	Yes:	No: <input checked="" type="checkbox"/>
Sampling, sale or offer to sell any product embodying the invention?	Yes:	No: <input checked="" type="checkbox"/>

If "yes" to any of the above, describe in detail the nature of such use, disclosure, sale, or offer to sell. Was the disclosure, if any, oral or written? Was it pursuant to a Non-Disclosure Agreement? Include names and dates:

.....

If "no" when do you expect any such use, disclosure, sampling or sale to occur? Please give details:

.....

13. PRIOR ART:

Please attach separate sheets describing the applicable prior art, including references to all pertinent prior art products, patents, and non-patent publications known to you: those of both STMicroelectronics and of any other company or person. Attach copies of all such literature that you are able to procure. APPLICANTS FOR A PATENT HAVE A DUTY TO DISCLOSE TO THE PATENT OFFICE ALL INFORMATION, OF WHICH THEY ARE AWARE, THAT IS MATERIAL TO THE EXAMINATION OF THE APPLICATION. FAILURE TO COMPLY WITH THAT DUTY OF DISCLOSURE IS A SERIOUS MATTER THAT MAY CAUSE THE PATENT APPLICATION TO BE PERMANENTLY STRICKEN.

An existing solution for applying low leakage vectors to a circuit is described in [1].

14. DESCRIPTION OF THE INVENTION

a. Problem solved by the invention:

A strong correlation has been shown to exist between the input vector applied to a logic cell and the leakage current through it [1, 2]. For example, for a 2-input static AND cell, it has been reported that the total drain to source leakage current when both the inputs are at logic 1 is 50 times greater than when the inputs are at logic 0 [2].

As process technologies continue to scale, leakage power becomes an increasingly important part of the total power dissipation of the chip. This is as threshold voltages and gate lengths are reduced in finer geometry processes, leading to increased leakage current. In addition, with gate oxide scaling significant leakage current starts to occur through the transistor gates. Leakage power is especially crucial in portable devices, such as cell phones, where it can directly affect after how long the device needs to be recharged.

This invention disclosure provides a mechanism by which a set of low leakages vectors can be applied to a circuit when its inputs are not changing. The idea is that during the sleep period a set of low leakage vectors are loaded into the flip-flops of the design by using the scan chain (after which the clock signal provided to the flip-flops can be shut-off). While some extra power is dissipated in loading the low leakage signals it should be remembered that even if the sleep period lasts several seconds, it could represent many billions of clock cycles. Across so many cycles the power dissipated in loading the low leakage vectors would pale in insignificance compared to the total leakage power.

b. Prior known solutions and their disadvantages (if available, attach copies of product literature, technical articles, patents, etc.). Why are these insufficient?

[REDACTED]

A solution for applying low leakage vectors starting at the latches of a design has been proposed in [1]. In [1] a "standby" signal is applied to all latches driving the circuit where leakage power dissipation is to be minimized. A determination is earlier made as to whether a logic 1 or logic 0 value at that latch output is likely to minimize leakage. Correspondingly, latches that enter a logic 1 or logic 0 value are used as needed.

Another techniques to reduce leakage power is to use large shut-off transistors which are provided to the power source. This technique requires significant layout overhead and also leads to power supply integrity issues [2].

- c. Advantages (technical and business) of the invention over what has been done before:

The solution presented in this invention disclosure has two advantages over that presented in [1]. These are:

(1) By using the existing scan chain in the design no modifications need to be made to the flip-flops or latches in the design. This means that there is no timing impact on the critical paths. Also there is no extra area or power overhead in having to use more complex flip-flops or latches

(2) By not routing the sleep signal (also referred to as the "standby" signal) to each flip-flop we avoid the area penalty, routing congestion and power dissipation in the design.

-
- d. Description of the construction and operation of the invention (attach, if necessary, appropriate schematic, block, timing diagrams; drawings; samples; graphs; flowcharts; computer listings; test results; etc.)

The idea behind the invention disclosure is shown in Figure 1. The invention disclosure allows us to re-use the scan chain in the design to supply low leakage vectors to the flip-flops. The scan chain is controlled by the TE (test-enable) signal which determines if the TI (test-in) input or standard D (data-in) input is loaded into each flip-flop.

In Figure 1 it can be seen that when the design enters a sleep or standby mode, the scan-chain is enabled by the LLE (low leakage enable) signal. This can be implemented by using a simple multiplexer. Also, the data inputted into the flip-flops through the scan chain is now the LLI (low-leakage input), instead of, the TI signal that is used during scan testing. This selection is also implemented with a multiplexer. Thus, a simple change at the input of the scan chain can allow to use the scan chain to load low leakage vectors in addition to scan testing.

The process of loading the low leakage vectors begins once a sleep signal is received. This sleep signal may be generated on-chip based on some time-out mechanism. Alternately, the signal could be provided from off-chip. In any case once it is received the LE signal needs to be invoked for every scan chain on chip. Before the LI vectors are scanned into the scan chain they must, however, be provided from a on-chip memory device or from off-chip. A finite state machine (FSM) ensures that the LLI inputs are serially available once the LE signal is turned on. In order to ensure that the right vectors are placed in each flip-flop the LE signal must be activated for only a number of cycles equal to the length of the scan chain. This will be controlled by the FSM. Since different scan chain in the design are likely to have different chain lengths the FSM must ensure that each scan chain will be only active for a specific number of cycles.

After the low leakage vector has been loaded the LE signals for each scan chain are turned off. Since there is no need to continue to clock the flip-flops now, the FSM controller then sends a clock gating signal to all clocks driving the scan chain flip-flops. This will lead to further power savings. The LLI vector applied to each scan chain will be pre-computed based on techniques presented in [2]. It is assumed that a fully automated flow mechanism will be provided by which a memory to hold the LLI vectors and FSM controller will be generated once the logic is known. This is necessary as the input vectors that cause minimal leakage current are strongly dependent on the logical structure of the module.

References

- [1] V. Dey et al, "Techniques for leakage power reduction," in Design of High-Performance Microprocessor Circuits, Edited by A. Chandrakasan, W. J. Bowhill, F. Fox, IEEE Press, 2001.
- [2] F. A. Aloul, S. Hassoun, K. A. Sakallah, D. Blaauw, "Robust SAT based serach algorithm for leakage power reduction," International Woksop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Sevilla, Spain 2002.
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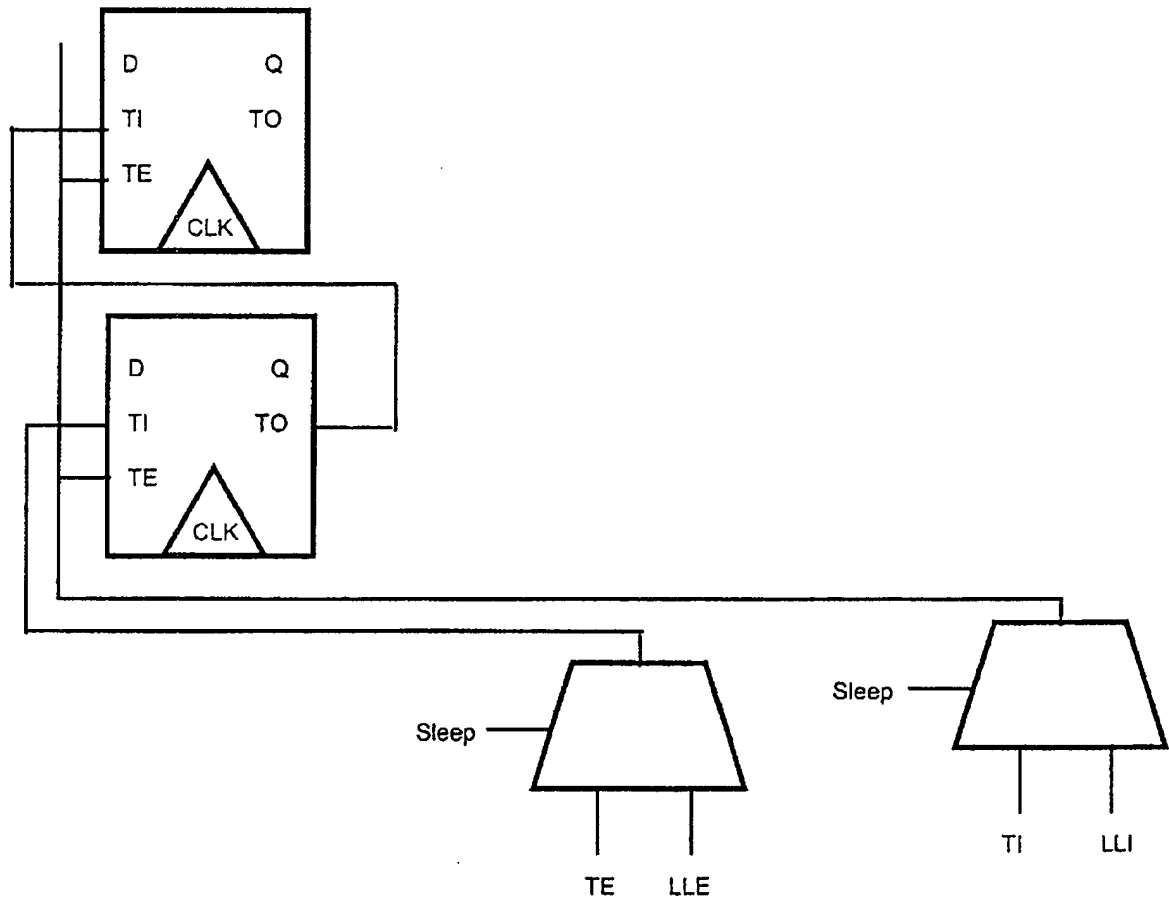


Figure 1: Illustrating the proposed leakage power reduction scheme using the scan chain.

If I do not agree that ST may pass upon request information relating to my last registered address to the Patent Attorney, I will let the IP department know by separate mail.

Inventor c): _____ Date: _____

We, the undersigned, have read and understood this disclosure:

Witness b) : _____ Date: _____

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MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

DECLARATION OF MARIO J. DONATO

1. This declaration is made in support of the accompanying Declaration of Prior Invention Under 37 CFR 1.131.

2. The person making this Declaration is Mario J. Donato.

3. I am currently employed in the Intellectual Property ("IP") department of STMicroelectronics, Inc. ("STMicroelectronics") as a Director, IP & Licensing, US & Asia, and have been employed by STMicroelectronics in this, or a similar, position since year 2000.

4. My responsibilities include the management of STMicroelectronics' patent portfolio, including the collection, review and approval of invention disclosures developed by employees of STMicroelectronics, and the preparation, prosecution and management of patent applications in the United States and foreign countries, as well as the management of outside law firms assigned to prepare and prosecution patent applications on behalf of STMicroelectronics.

5. Attached is a true and correct copy of the following documents included within STMicroelectronics patent application file(s) for the above-identified U.S. patent application:

Letter dated March 6, 2003 (from STMicroelectronics to an outside law firm authorizing/instructing the preparation and filing of a patent application for Invention Disclosure No. 03-LJ-011, entitled "Scan Chain Modification For Reduced Leakage Power Dissipation

6. The IP department of STMicroelectronics receives a significant number of invention disclosures from STMicroelectronics employees at various times throughout the year. After a short period of time (usually from one to two months), the received invention disclosures are reviewed by one or more persons in the IP department, or by a committee. Upon, or after review, a particular invention disclosure may be approved for filing of a patent application (in the U.S. and/or other foreign country). The approval process generally may be done immediately after review, or may take a short period of time (usually from one to two months) depending on the approvals necessary (which may include additional approvals based upon budget, manpower, and/or other organizational and business factors).

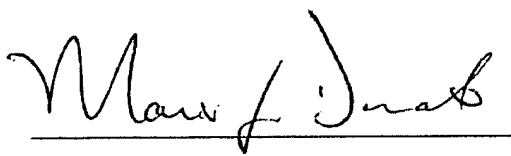
7. Once the approval process is completed, the invention disclosure is assigned to either in-house counsel or an outside law firm for preparation and filing. For this application, it was assigned to outside counsel for preparation. The time period necessary to prepare and file a

patent application after final approval of invention disclosure is usually based upon several factors, such as the workloads of the in-house patent attorney or agent managing the application and the outsourced law firm preparing and filing the application, time of year, the availability and work demands of the inventor(s), and other business factors.

8. As a person signing below:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE:

A handwritten signature in black ink, appearing to read "Mario J. Donato", is written over a horizontal line.

Mario J. Donato
Director, IP & Licensing, US & Asia



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March 6, 2003

Richard A. Bachand, Esq.
Bachand Law Office
5353 Wyoming Blvd., N.E., Suite 3
Albuquerque, NM 87109-3132

Re: Patent Disclosures Entitled:

[REDACTED]

[REDACTED]

Scan Chain Modification to Support Reduced Leakage Power Dissipation
Our File No. 03-LJ-011

[REDACTED]

Dear Rich:

The STMicroelectronics Patent Committee met on January 24, 2003 at which time a decision was made to file patent applications on the above-referenced disclosures. Please proceed to prepare and file the applications within ninety (90) days, or earlier if possible. A copy of each disclosure is enclosed for your reference.

[REDACTED]

Richard A. Bachand
March 6, 2003
Page 2

If you have any questions, do not hesitate to contact me at (972) 466-7503.

Very truly yours,



Mario J. Donato, Jr.
Intellectual Property & Licensing Attorney

mh

Enclosure



STMicroelectronics, Inc.



ST003-CARR/10

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